VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) An apparatus comprising:

a phase lock loop (PLL) configured to multiply an input frequency to generate an output frequency in response to a multi-bit lock signal; and

a lock circuit configured to generate said multi-bit lock signal, wherein said PLL is configured to (i) (a) select a reference frequency as [(i)] said input frequency and (b) select a first feedback ratio, when in a first mode and (ii) (a) select a divided frequency of said input frequency as said input frequency and (b) select a second feedback ratio, when in a second mode, wherein a first bit of said multi-bit lock signal selects said first feedback ratio and a second bit of said multi-bit lock signal selects said second feedback ratio.

2. (AMENDED) The apparatus according to claim 1, wherein said first mode is further configured to increase [a] said first feedback [divide] ratio.

3. (AMENDED) The apparatus according to claim 2, wherein said second mode is further configured to decrease said second feedback [divide] ratio.

6. (AMENDED) The apparatus according to claim 1, wherein said lock [circuit] signal is [configured] generated in further response to an internal/external signal.

8. (AMENDED) The apparatus according to claim 1, wherein said multi-bit lock is externally controlled by a user.

10. (AMENDED) The apparatus according to claim 9, wherein said first and second switchable dividers are further configured in response to said multi-bit lock signal.

11. (AMENDED) The apparatus according to claim 10, wherein:

said first switchable divider comprises a first divider and a first multiplexer, wherein said first multiplexer is configured to select a first divided output frequency or said input frequency [and present] as said reference frequency; and

said second switchable divider comprises a second divider, a third divider and a second multiplexer, wherein said multiplexer is configured to select a second divided output frequency or a third divided frequency [and present] as said feedback frequency.

14. (AMENDED) The apparatus according to claim 11, wherein said second and third dividers comprise multi-channel dividers configured in response to said multi-bit lock signal.

15. (AMENDED) An apparatus comprising:

means for multiplying an input frequency in response to a lock signal;

means for generating an output frequency in response to said input frequency;

means for generating said lock signal; and

means for (i) (a) selecting said input frequency to be a reference frequency and (b) selecting a first feedback ratio, when in a first mode and (ii) (a) selecting a divided frequency of said input frequency to be said reference frequency and (b) selecting a second feedback ratio, when in a second mode, wherein a first bit of said multi-bit lock signal selects said first feedback ratio and a second bit of said multi-bit lock signal selects said second feedback ratio.

16. (AMENDED) A method for frequency and/or phase acquisition in a phase lock loop (PLL), comprising the steps of:

(A) multiplying an input frequency in response to a lock signal;

(B) generating said lock signal [by];

(C) (i) (a) selecting said input frequency to be [(i)] a reference frequency and (b) selecting a first feedback ratio, when in a first mode and (ii) (a) selecting a divided frequency of said input frequency to be said reference frequency and (b) selecting a second feedback ratio, when in a second mode, wherein a first bit of said multi-bit lock signal selects said first feedback ratio and a second bit of said multi-bit lock signal selects said second feedback ratio.

17. (AMENDED) The method according to claim 16, wherein step (A) further comprises:

increasing [a] said first feedback [divide] ratio when in said first mode; and

decreasing said second feedback [divide] ratio when in said second mode.

18. (AMENDED) The method according to claim 16, wherein step (B) [is further configured] generates said lock signal in further response to an internal/external signal.

21. (NEW) An apparatus comprising:

a phase lock loop (PLL) configured to multiply an input frequency to generate an output frequency in response to a lock signal; and

a lock circuit configured to generate said lock signal in response to an external input, wherein said PLL is configured to (i) select a reference frequency as said input frequency when in a first mode and (ii) select a divided frequency of said input frequency as said input frequency when in a second mode, wherein either said first mode or said second mode is selected in response to said lock signal.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

INFORMATION DISCLOSURE STATEMENT

A copy of the 1449 filed January 11, 2002 is included, along with the cited reference, with this response since the 1449 was previously cited and apparently misplaced.

IN THE DRAWINGS

While Applicants' representative does not necessarily agree with the requirement to label FIG. 1, in order to further prosecution, FIG. 1 has been labeled "conventional". As such, the objection to the drawings should be withdrawn.

SUPPORT FOR CLAIM AMENDMENTS

Support for the feedback ratios can be found on page 11, lines 14-21. Support for the multi-bit lock signal can be found on page 7, lines 11-14. As such, no new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-12 and 14-20 under 35 U.S.C. §102 as being anticipated by Gotz et al. (German Patent No.

19946200A1) has been obviated by appropriate amendment and should be withdrawn.

Gotz discloses a circuit with a PFD and a VCO (FIG. 1 of Gotz).

In contrast, claims 1, 15 and 16 of the present invention provide a first mode that selects a first feedback ratio and a second mode that selects a second feedback ratio in response to a multi-bit lock signal. From the figures, Gotz does not appear to disclose or suggest such a multi-bit lock signal. However, a translation has not been provided. Applicants' representative asks that the Examiner obtain a translation. If no new information is revealed, claims 1, 15 and 16 are believed to be patentable over Gotz and the rejection should be withdrawn.

Furthermore, claim 14 provides that the second and third dividers comprise multi-channel dividers configured in response to the lock signal. Gotz does not disclose or suggest such multi-channel dividers. As such, claim 14 is independently patentable over Gotz and the rejection should be withdrawn.

Newly presented claim 21 provides a lock circuit that may be configured to generate a lock signal in response to an external input. A PLL may also be configured to select a reference frequency as (i) the input frequency when in a first mode and (ii) a divided frequency of the input frequency when in a second mode, where either the first or second mode is selected in response to

the lock signal. Gotz does not disclose or suggest such a lock signal generated in response to an external input, as presently claimed.

In particular, the output of the control logic of Gotz (the so-called lock signal) is presented to the MUX1 and MUX2. However, the control logic of Gotz only responds to an internal signal received (indirectly) from the phase detector through the block marked "US". Therefore, Gotz does not respond to an external signal, as presently claimed. As such, Gotz does not disclose or suggest each and every element of the presently claimed invention and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 13 under 35 U.S.C. §103 as being unpatentable over Gotz is respectfully traversed and should be withdrawn. Claim 13 indirectly depends from claim 1, which is now believed to be allowable.

The rejection of claims 5, 7 and 8 under 35 U.S.C. §103 as being unpatentable over Gotz, in view of Lada, is respectfully traversed and should be withdrawn. Claims 5, 7 and 8 depend from claim 1, which is now believed to be allowable.

As such, the presently claimed invention is fully patentable over the cited references and the rejection should be allowable.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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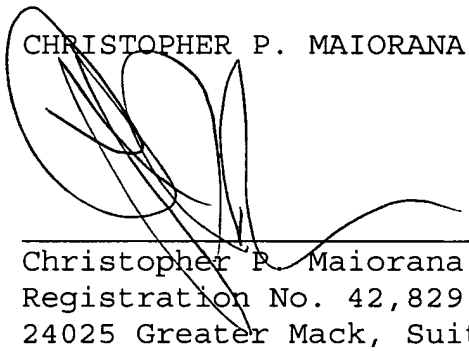

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